REMARKS

Claims 1-18 were pending in the above-identified application; of these, claims 1-9 are rejected, claims 5 and 7 objected to, and claims 10-18 cancelled in response to a restriction requirement. Applicant respectfully requests reconsideration.

Election/Restrictions

The Examiner subjected claims 1-18 to a restriction requirement. Applicant provisionally elected to prosecute claims 1-9, and hereby affirms that election.

Rejections Under 35 U.S.C. 102

Claims 1-4, 6, 8, and 9

Claims 1-4, 6, 8, and 9 stand rejected under section 102(b) as anticipated by Honda et al. (5,497,109). These rejections are traversed in view of the following remarks.

To reject a claim as anticipated under section 102, the Examiner must show where *every* element of the claim is explicitly or impliedly taught in a cited reference.

> [F]or anticipation under 35 U.S.C. 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present.

(MPEP 706.02, 700-21, February 2003.) A claim rejection under section 102 should therefore be withdrawn if the cited reference fails to teach even a single aspect of the claim.

Claim 1

The Examiner cited Honda's col. 1, lines 21-29, and Figure 1 as teaching every element of claim 1 (OA, page 3). As characterized by Honda, that Figure 1 depicts a "clock distribution system" (Honda, col. 1, lines 15-27).

Claim 1 recites a "method of measuring signal skew". Honda et al. may suggest minimizing skew, but the Examiner

points to nothing in Honda et al. that teaches any method of measuring skew, much less the method of claim 1. This essential difference between the teachings of Honda et al. and Applicant's claims is one of many reasons the rejection of claim 1 should be withdrawn. The following is a non-exhaustive list of other important distinctions between claim 1 and the referenced teachings of Honda et al.:

1. The claimed method is employed to measure skew "on a programmable logic device," the programmable logic device including "programmable logic blocks" that are "programmably connectable to…destination branches" of a signal tree (claim 1). Honda et al. does not teach a "programmable logic device" (see Applicant's paragraph **[0002]** for an explanation of the term), and the Examiner has not identified any teaching in Honda et al. of programmable logic blocks, or blocks that are programmably connectable to a signal tree.
2. The skew measurement technique of claim 1 includes "instantiating a first delay element on the device using a first programming sequence" and "instantiating a second delay element on the device using a second programming sequence…" As is commonly known to those familiar with programmable logic devices, circuits are instantiated in programmable logic "by loading configuration data into internal configuration memory cells that define how the [configurable logic blocks], interconnections, and [input/output blocks] are configured" (Applicant's specification, paragraph **[0002]**). Applicant's Figures 2 and 3 provide support for the claimed first and second delay elements instantiated in programmable logic. Honda et al. does not teach a programmable logic device, and so

cannot be said to teach "instantiating" delay elements as claimed.

Any one of the foregoing distinctions is sufficient to overcome the rejection of claim 1 or Honda et al. The rejection of claim 1 should therefore be withdrawn.

Claims 2, 3, 4, 6, 8, and 9

Claims 2-4, 6, 8, and 9 depend from claim 1, and therefore distinguish Honda et al. for at least the same reasons claim 1 distinguishes. The rejections of claims 2, 3, 4, 6, 8, and 9 should therefore be withdrawn.

Claim 6 adds to the method of claim 1 a number of programming sequences that instantiate third and fourth delay elements in programmable logic. The Examiner rejects claim 6 over Honda et al., once again pointing to Figure 1 of that reference. However, Applicant finds nothing in Figure 1 of Honda et al. that teaches the claimed method.

With respect to claim 8, the Examiner states "Honda et al. … teaches that configuring the device to include the first and second delay elements in respective first and second oscillators. (311; See figure 2)" (OA, page 4). In referring to figure 2 of Honda et al., Applicant finds nothing to support the Examiner's assertion. Where is the device configured to include delay elements? Where are the first and second oscillators that incorporate these delay elements? In the absence of such teaching, the rejection of claim 8 should be withdrawn.

In rejecting claim 9, the Examiner asserts that Honda et al. teach "comparing the periods of the first and second oscillators," citing Figure 6 of Honda et al. (OA, page 4). Figure 6 of Honda et al. is "a timing chart for explaining clock driver operations" (Honda et al., col. 8, lines 22-23). Figure 6 of Honda et al. appears to have nothing to do with a method of measuring skew, makes no reference to first and second oscillators, and does not compare the periods of two

oscillators. The rejection of claim 9 should therefore be withdrawn.

Claim Objections

Claim 5 is objected to for reciting a "second logic block" between "first and second logic blocks." Claim 5 is amended to recite a "second logic block … physically between the first and ~~second~~ third logic blocks." Applicant is grateful for the Examiner's attention to detail, and has amended claim 5 to correct the identified inadvertent error.

Claim 5, as amended, remains dependent from claim 1, and therefore distinguishes Honda at al. for at least the same reasons claim 1 distinguishes.

Claim 7 is objected to as being dependant upon a rejected base. Claim 7 depends from claims 6 and 1, and therefore distinguishes Honda et al. for at least the same reasons those claims distinguish.

New Claims

Applicant added new claims 19-26, each of which is supported by the specification and allowable over the cited references. No new matter is added.

CONCLUSION

For the reasons presented above, the pending claims are in condition for allowance; accordingly, Applicant respectfully requests a Notice of Allowance. If the Examiner's

next action is other than allowance of the pending claims, the Examiner is requested to call Applicant's representative at (408) 879-4641.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, Mail Stop NON-FEE AMENDMENT, on September 15 , 2003.

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Name

Signature